Remarks

The Final Office Action dated October 24, 2008, lists the following rejection: claims 1-7 stand rejected under 35 U.S.C. § 103(a) over Schmoock *et al.* (US 6,624,994) in view of Valley (U.S. 4,743,779) and Applicant's Figure 1. In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in the instant Office Action unless Applicant expressly indicates otherwise.

Applicant further traverses the § 103(a) rejection of claims 1-7 because the modification of the '994 reference in view of Applicant's Figure 1 proposed by the Examiner undermines a stated purpose of the '994 reference. *See, e.g.,* M.P.E.P. § 2143.01 "If (a) proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.". S*ee also In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984). The Examiner asserts that the '994 reference discloses a comparator (*i.e.,* element 40 of Figure 2) that compares the voltage of the source of transistor 32 to the voltage of the source of transistor 52; however, the Examiner acknowledges that the '994 reference does not teach that this "comparator" outputs a low-current signal when the magnitude of the voltage across the main cell outputs falls below that across the sense cell outputs as in the claimed invention. The Examiner then proposes modifying the '994 reference's operational amplifier 40 such that it outputs a low-current signal. Applicant submits that such a modification would render the '994 reference unsatisfactory for its stated purpose of providing an over-current protection scheme that protects switch transistor 32. *See, e.g.,* Figure 2 and Col. 5:8-11. Specifically, the '994 reference's operational amplifier 40 adjusts its output signal in relation to the differential signal at its inputs in order to cause the source voltages of transistors 32 and 52 to be relatively equal, thereby providing over-current protection. *See, e.g.,* Figure 2 and Col. 6:35-50. The Examiner's proposed modification would alter the '994 reference's operational amplifier 40 such that it would output a low-current signal (responsive to the voltages on the outputs of the transistors 32 and 52), instead of adjusting its output signal to control the source voltages of the transistors 32 and 52 as required by the '994 reference to provide over-current protection. Applicant submits that the '994 reference's operational amplifier 40 would no longer provide over-current protection, thus rendering the '994 reference unsatisfactory for its

stated purpose. As such, there is no motivation for the skilled artisan to modify the '994 reference in the manner proposed by the Examiner.

On page 3:5-13 of the instant Office Action, the Examiner appears to be confusing the level of the signal output by operational amplifier 40 (*e.g.,* a low output) with what kind of output signal is being produced by the operational amplifier 40 (*i.e.,* an output signal that controls the source voltages of the transistors 32 and 52). Applicant submits that a low (level) output signal is not equivalent to a low-current signal (which could be a low level or a high level signal) that is produced responsive to comparing the voltages across main cell and sense cell outputs. Irrespective of the level of the output signal generated by operational amplifier 40, the Examiner's proposed modification would result in operational amplifier 40 generating a low-current signal responsive to comparing the voltages on the outputs of the transistors 32 and 52, instead of adjusting its output signal in relation to the differential signal at its inputs in order to cause the source voltages of transistors 32 and 52 to be relatively equal. As such, the Examiner's proposed modification would render the '994 reference unsatisfactory for its intended purpose of providing over-current protection using operational amplifier 40.

In view of the above, there is no motivation for the skilled artisan to modify the '994 reference in the manner proposed by the Examiner. Accordingly, the § 103(a) rejection of claims 1-7 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 103(a) rejection of claims 1-7 because the cited combination does not correspond to the claimed invention which includes, for example, aspects directed to comparing the voltages across the main cell controlled outputs and the sense cell controlled outputs and outputting a low-current signal when the magnitude of the voltage across the main cell controlled outputs falls below that across the sense cell controlled outputs. The Examiner acknowledges that the '994 and '779 references fail to disclose a comparator that outputs a low-current signal as in the claimed invention. The Examiner then cites to the comparator 18 of Applicant's Figure 1 (admitted prior art); however, the comparator 18 does not compare the voltages across main cell outputs and sense cell outputs because Figure 1 does not have main cell outputs and sense cell outputs. *See, e.g.,* Applicant's Figure 1. As such, the Examiner fails to cite to any reference that teaches or suggests a comparator that compares the voltages across the

main cell controlled outputs and the sense cell controlled outputs and that outputs a low-current signal as in the claimed invention. The Examiner, in the last paragraph beginning on page 3 of the instant Office Action, acknowledges that none of the cited references teach these aspects of the claimed invention. Instead the comparator 18 of AAPA was merely used "to show that (it) is known to use a comparator to output a low-current signal when the magnitude of the voltage across a cell output falls below a value." Applicant submits that the Examiner has tacitly acknowledged that AAPA is not being combined with the '994 reference in the manner taught by the references (*i.e.,* to compare the output of transistor 32 to a reference value), but instead to compare the output of transistor 32 to the output of transistor 52. Thus, the Examiner has simply identified elements and appears to be arranging these elements, not in the manner taught by the cited references, but in the manner taught by the claimed invention, which is a hallmark of improper hindsight reconstruction. *See, e.g.,* M.P.E.P. § 2142. Accordingly, the § 103(a) rejection of claims 1-7 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the § 103(a) rejection of claims 1-7 because the Examiner fails to provide sufficient detail regarding the proposed combination of the '994 and '779 references to enable Applicant to determine the propriety of such a combination. Applicant notes that while the Examiner has identified the elements of the cited references, little explanation of how these elements are combined is provided. In order to comply with 35 U.S.C. § 132, sufficient detail must be provided by the Examiner regarding the alleged correspondence between the claimed invention and the cited reference to enable Applicant to adequately respond to the rejections. *See, also,* 37 CFR 1.104 ("The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.") and M.P.E.P. § 706.02(j), ("It is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply.").

Applicant previously requested that the Examiner provided clarification regarding how the cited references are being combined, and while Applicant appreciates the Examiner's clarification that the '994 reference's feedback circuit (*i.e.,* elements V_{ref}, 44 and 48 of Figure 2) is being modified to provide both over-current protection and under-voltage protection, the Examiner still has not provided any detail regarding how the '994

reference's feedback circuit is to be modified. The Examiner acknowledges that the feedback circuit of the '779 reference provides over-voltage and under-voltage protection, not over-current protection and under-voltage protection as the '994 reference's feedback circuit is apparently being modified (in some undisclosed manner) to provide. As such, it is unclear from the cited portions the '994 and '779 references how the Examiner is modifying the feedback circuit of the '994 reference to provide two different protection schemes that are not taught as being provided together by the feedback circuits of either reference. Applicant submits that the Examiner has simply identified elements from the '994 and '779 references and improperly concluded that these elements can be combined in some unidentified manner. *See, e.g.,* M.P.E.P. § 2142 ("rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."). Without further clarification regarding how the cited portions of the '994 and '779 references are being combined, the § 103(a) rejection of claims 1-7 is improper and cannot be maintained.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: _____
Name: Robert J. Crawford
Reg. No.: 32,122
651-686-6633
(NXPS.539PA)